35 U.S.C. § 102 Rejections

The Examiner has rejected claims 1-9, 16,17 and 19, 20 under 35, U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,991,199 to Brigati et al. *See Examiner's Office Action* p.7 (03 July 2002).

With respect to Independent Claim 1, Examiner has stated that "Claim 1 is rejected under 35 U.S.C. 102(e) as being clearly anticipated by Brigati.... (Brigati, especially Fig. 1-3 and Col. 5, line 60 to Col. 8, line 35)." *See Examiner's Office Action* p.7 (03 July 2002).

Applicant respectfully asserts that Brigati does not anticipate Applicant's Claim 1. Applicant's Claim 1 recites

> 1. An emulated EEPROM memory device, comprising a memory macrocell which is embedded into an integrated circuit having a microcontroller, **the memory macrocell including a Flash memory structure formed by a predetermined number of sectors**, wherein **at least two sectors of the Flash memory structure** are structured to **emulate EEPROM byte alterability**. (emphasis added).

Applicant respectfully disagrees with Examiner that Brigati shows or suggests the recitations of Applicant's Claim 1. Rather, on its face Brigati claims methods and systems for "programming of flash-EPROM" type memory cells, and does not show or suggest the recitations of Applicant's Claim 1 (especially the foregoing bolded portions Claim 1). *See Brigati* cols. 8-14. In addition, Applicant has reviewed the portion of Brigati cited by Examiner, Fig. 1-3 and Col. 5, line 60 to Col. 8, line 35, and cannot discern where Brigati shows or describes "**... a Flash memory structure** formed by a predetermined number of sectors, wherein **at least two sectors of the Flash memory structure** are **structured to emulate EEPROM byte alterability**," as recited by Applicant's Claim 1. Instead, the text cited by Examiner seems to support the claims of Brigati for methods and systems for "programming of flash-EPROM" type memory cells. Indeed, Applicant has electronically searched the text of Brigati and has found no instance in Brigati which describes any "**sectors of ... memory structure** ... structured to **emulate EEPROM byte alterability"** (let alone especially using a "Flash memory structure"). Hence, Applicant can not at all see how Brigarti is at all relevant to Applicant's Claim 1. Accordingly, for at least the foregoing reasons, Applicant respectfully suggests that Brigati does not establish a prima facie case of anticipation Applicant's Claim 1, and respectfully requests the

Examiner to withdraw his rejection and issue a Notice of Allowance of Independent Claim 1. In addition, Dependent Claims 2-7 depend either directly or indirectly from Independent Claim 1. "A claim in dependent form shall be construed to incorporate by reference all the limitations of the claim to which it refers." 35 U.S.C. § 112 paragraph 4. Consequently, Dependent Claims 2-7 are not anticipated by the art of record for at least the reasons why Independent Claim 1 is not anticipated by the art of record. Accordingly, Applicant respectfully requests that Examiner withdraw his rejections of Dependent Claims 2-7 for at least these reasons, and issue a Notice of Allowance on such dependent claims.

With respect to Independent Claim 8, Examiner has stated that "Claim 8 is rejected under 35 U.S.C. 102(e) as being clearly anticipated by Brigati.... (Brigati, especially Fig. 1-3 and Col. 7, line 65 to Col. 8, line 40 and Col. 11, line 62 to Col. 12, line 8)." *See Examiner's Office Action* p.9 (03 July 2002). In response to Examiner, Applicant has amended Claim 8 to be Applicant's Claim 9 rewritten in independent form such that herein amended Independent Claim 8 currently reads

> 8. A method for emulating features of an EEPROM memory device incorporated into a memory macrocell which is embedded into an integrated circuit that also includes a microcontroller and a Flash memory structure formed by a predetermined number of sectors, comprising using at least two sectors of the Flash memory structure to emulate EEPROM byte alterability by dividing each of said at least two sectors into a pre-determined number of blocks of the same size and each block into a pre-determined number of pages and updating the emulated EEPROM memory portion programming different memory locations in a single bit mode, wherein at a page update selected page data are moved to a next free block and, when an EEPROM sector is full, all the pages are swapped to another EEPROM sector.

With respect to previously unamended Dependent Claim 9, Examiner has stated that "in regards to Claim 9, the method according to Claim 8, wherein at a page update selected page data are moved to a next free block and, when an EEPROM sector is full, all the pages are swapped to the another EEPROM sector, is taught by Brigati (especially Fig. 1-3 and Col. 7, line 65 to Col. 8, line 40 and Col. 11, line 62 to Col. 12, line 8)." *See Examiner's Office Action* p.9 (03 July 2002). Applicant respectfully disagrees that Brigati shows or suggests herein amended Claim 8 (which is previous Claim 9 rewritten in independent form), With respect to the cited portions of Brigati, Brigati states as follows

The programming of the memory array of the memory 1 is achieved by a sequence of operations.

During a first operation, the cells such as 2 to 9 of a first page are selected by means of the command applied on the connection 71 of the multiplexing circuit 33.

Then, preferably, during a second operation, all the cells 2 to 9 of the same page are programmed at the same level making it possible to obtain a uniform threshold voltage for each cell of the selected page. During a third operation, all the selected cells 2 to 9 are erased. During the erasure, the bias voltage applied to the control gate electrode of a word 10 is in the range of -6V. All the cells of the same word line such as 30 receive this voltage whether or not the page is selected. Furthermore, the source electrode is taken to a voltage of about 10V. The drain electrode is taken to a state of high impedance. The erasure requires a series of several very brief pulses of about 100 .mu.s. These voltages, during erasure, may prompt firstly a depletion in the cells such as 2 to 9 of the selected page. The cells such as 35 of a non-selected page furthermore receive this same voltage of -6V at their control gate electrode. This negative voltage causes losses of charges at their floating gate and tends to erase them to some extent.

For selected cells such as 2 to 9 of a selected page, it is ascertained before any programming, according to the invention, that the cells have undergone a depletion. If this is the case, these cells are reprogrammed slightly so that they recover a threshold voltage that has become excessively low after erasure. Similarly, a reprogramming or refreshing operation will be done on the non-selected cells such as 35 of a non-selected page that may have undergone a parasitic erasure or a loss of charges during the erasure preceding the programming owing to the high voltage applied to the word line such as 30.

Brigati, col. 7, line 65 to col. 8, line 40.

successively programming a first page and a second page of the memory array of the memory, the first page being programmed during a first instruction and the second page during a second instruction.

14. The method of claim 12, wherein:

the memory array of the memory is organized into two distinct pages, a first page and a second page, both consisting of groups of vertically adjacent words, the two pages together comprising horizontally interleaved words of this kind,

successively programming a first page and a second page of the memory array of the memory, the first page being programmed during a first instruction and the second page during a second instruction.

Brigati, col. 11, line 62 to col. 12., line 8.

Applicant respectfully points out, so far as Applicant can tell, the foregoing-cited portions of Brigati did not show or suggest the recitations of the previously unamended Claim 8, and consequently surely do not show or suggest a "**...using at least two sectors of the Flash memory structure to emulate EEPROM byte alterability by dividing each of said at least two sectors into a pre-determined number of blocks of the same size and each block into a pre-determined number of pages and updating the emulated EEPROM memory portion** programming different memory locations in a single bit mode, **wherein at a page update selected page data are moved to a next free block and, when an EEPROM sector is full, all the pages are swapped to another EEPROM sector,**" as recited by Applicant's Claim 8 (especially the foregoing bolded portions of Claim 8). Accordingly, for at least the foregoing reasons, Applicant respectfully suggests that Brigati both did not and does not establish a prima facie case of anticipation of Applicant's Independent Claim 8, and respectfully requests that Examiner issue a Notice of Allowance for Claim 8.

With respect to Independent Claim 16, Examiner has stated as follows:

> Claim 16 is rejected under 35 U.S.C. 102(e) as being clearly anticipated by Brigati.
>
> 16. A method of emulating an EEPROM using Flash memory, the method comprising:
>
> dividing the Flash memory into first and second memory sectors each including a plurality of memory blocks, each memory block including plural memory pages each with plural memory locations (Brigati, especially Fig. 1-3 and Col. 7, line 65 to Col. 8, line 40 and col. 11, line 62 to col. 12, line 8);
>
> assigning to each memory page of the first and second memory sectors a page address that is shared by a corresponding page in each of the memory blocks of the first and second memory sectors (Brigati, especially Fig. 1-3 and Col. 7, line 65 to Col. 8, line 40 and col. 11, line 62 to col. 12, line 8);
>
> in response to a first write instruction to write to a selected page address, writing to a data page of a first memory block of the first memory sector (Brigati, especially Fig. 1-3 and Col. 7, line 65 to Col. 8, line 40 and col. 11, line 62 to col. 12, line 8); and
>
> in response to a second write instruction to write data to the selected page address, writing to a data page of a second memory block of the first memory sector

(Brigati, especially Fig. 1-3 and Col. 7, line 65 to Col. 8, line 40 and col. 11, line 62 to col. 12, line 8)." *See Examiner's Office Action* p.10 (03 July 2002).

With respect to the Examiner-cited portions of Brigati, Applicant respectfully points out that those cited portions state as follows

> The programming of the memory array of the memory 1 is achieved by a sequence of operations.
>
> During a first operation, the cells such as 2 to 9 of a first page are selected by means of the command applied on the connection 71 of the multiplexing circuit 33.
>
> Then, preferably, during a second operation, all the cells 2 to 9 of the same page are programmed at the same level making it possible to obtain a uniform threshold voltage for each cell of the selected page. During a third operation, all the selected cells 2 to 9 are erased. During the erasure, the bias voltage applied to the control gate electrode of a word 10 is in the range of -6V. All the cells of the same word line such as 30 receive this voltage whether or not the page is selected. Furthermore, the source electrode is taken to a voltage of about 10V. The drain electrode is taken to a state of high impedance. The erasure requires a series of several very brief pulses of about 100 .mu.s. These voltages, during erasure, may prompt firstly a depletion in the cells such as 2 to 9 of the selected page. The cells such as 35 of a non-selected page furthermore receive this same voltage of -6V at their control gate electrode. This negative voltage causes losses of charges at their floating gate and tends to erase them to some extent.
>
> For selected cells such as 2 to 9 of a selected page, it is ascertained before any programming, according to the invention, that the cells have undergone a depletion. If this is the case, these cells are reprogrammed slightly so that they recover a threshold voltage that has become excessively low after erasure. Similarly, a reprogramming or refreshing operation will be done on the non-selected cells such as 35 of a non-selected page that may have undergone a parasitic erasure or a loss of charges during the erasure preceding the programming owing to the high voltage applied to the word line such as 30.
>
> *Brigati*, col. 7, line 65 to col. 8, line 40.

successively programming a first page and a second page of the memory array of the memory, the first page being programmed during a first instruction and the second page during a second instruction.

14. The method of claim 12, wherein:

the memory array of the memory is organized into two distinct pages, a first page and a second page, both consisting of groups of vertically adjacent words, the two

pages together comprising horizontally interleaved words of this kind,

successively programming a first page and a second page of the memory array of the memory, the first page being programmed during a first instruction and the second page during a second instruction.

Brigati, col. 11, line 62 to col. 12., line 8.

Applicant respectfully points out that, so far as Applicant can tell, the foregoing-cited portions of Brigati do not show or suggest a "dividing the Flash memory into first and second memory sectors each including a plurality of memory blocks, each memory block including plural memory pages each with plural memory locations," as recited by Applicant's Claim 16. Rather, as set forth above, Brigati recites "during a first operation, the cells such as 2 to 9 of a first page are selected by means of the command applied on the connection 71 of the multiplexing circuit 33," which does not match the immediately foregoing-cited recitations of Applicant's Claim 16. In addition, as far as Applicant can tell, the above set forth portions of Brigati do not show or suggest "assigning to each memory page of the first and second memory sectors a page address that is shared by a corresponding page in each of the memory blocks of the first and second memory sectors," as recited by Applicant's Claim 16. Rather, as set forth above, Brigati recites "during a second operation, all the cells 2 to 9 of the same page are programmed at the same level making it possible to obtain a uniform threshold voltage for each cell of the selected page," which does not match the foregoing-cited recitations of Applicant's Claim 16. In addition, as far as Applicant can tell, the foregoing-cited portions of Brigati do not show or suggest "in response to a first write instruction to write to a selected page address, writing to a data page of a first memory block of the first memory sector," as recited by Applicant's Claim 16. Rather, as set forth above above, Brigati recites "during a third operation, all the selected cells 2 to 9 are erased," which does not match the foregoing-cited recitations of Applicant's Claim 16. In addition, as far as Applicant can tell, the foregoing-cited portions of Brigati do not show or suggest "in response to a second write instruction to write data to the selected page address, writing to a data page of a second memory block of the first memory sector," as recited by Applicant's Claim 16. Rather, as recited above, Brigati recites "for selected cells such as 2 to 9 of a selected page, it is ascertained before any programming,

according to the invention, that the cells have undergone a depletion.... if this is the case, these cells are reprogrammed slightly so that they recover a threshold voltage that has become excessively low after erasure.... similarly, a reprogramming or refreshing operation will be done on the non-selected cells such as 35 of a non-selected page that may have undergone a parasitic erasure or a loss of charges during the erasure preceding the programming owing to the high voltage applied to the word line such as 30," which does not match the foregoing-cited recitations of Applicant's Claim 16.

As has been shown, Brigati does not show or suggest any of the recitations of Applicant's Independent Claim 16. Accordingly, for at least the foregoing reasons, Applicant respectfully suggests that Brigati does not establish a prima facie case of anticipation of Applicant's Independent Claim 16, and respectfully requests the Examiner issue a Notice of Allowance for Claim 16. In addition, Claims 17-20 depend either directly or indirectly from Independent Claim 16. "A claim in dependent form shall be construed to incorporate by reference all the limitations of the claim to which it refers." 35 U.S.C. § 112 paragraph 4. Consequently, Dependent Claims 17-20 are not anticipated by the art of record for at least the reasons why Independent Claim 16 is not anticipated by the art of record. Accordingly, Applicant respectfully requests that Examiner with his rejection of Dependent Claims 17-20 for at least these reasons, and issue a Notice of Allowance on such dependent claims.

35 U.S.C. § 103 Rejections

Examiner has stated that "Claims 10-12, and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Devin in view of Cappelletti. *See Examiner's Office Action* pp.11 (03 July 2002).

With respect to Independent Claim 10, Examiner has stated that "Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Devin in view of Cappelletti.... Devin teaches the use of a Flash memory device, and first and second memory portions for programming the device. However, Devin does not expressly teach the use of pointers for reading and writing to memory locations. Cappelletti does expressly teach the use of pointers when programming the memory portions of a Flash memory device (see Col. 2, lines 50-60). It would have been obvious to one of ordinary skill in the art at the time the invention was made to

modify the teachings of Devin with Cappelletti because doing so optimizes the programming of flash memory devices." *See Examiner's Office Action* p.12 (03 July 2002).

Applicant respectfully disagrees with Examiner that Devin in view of Cappelletti shows or suggests the recitations of Applicant's Independent Claim 10. As noted by Examiner, Applicant's Independent Claim 10 recites

> 10. A Flash memory device for emulating an EEPROM, comprising:
>
> first and second Flash memory portions each including plural memory blocks with plural memory locations, each of the memory locations sharing an address with a corresponding memory location in each of the blocks of the first and second Flash memory portions, all of the memory locations sharing a same address being a set of memory locations; and
>
> a plurality of memory pointers each reflecting which memory block includes a current memory location for a set of memory locations, each set of memory locations including a current memory location; and
>
> a memory controller structured to, in response to receiving a request to write data to a selected address assigned to a selected one of the sets of memory locations, determine from a memory pointer associated with the selected address which memory location in the selected set is a next memory location following the current memory location for the selected set and write the data in the next memory location.

Applicant respectfully points out that, while Examiner has graciously cited the recitations of Applicant's Claim 10, Examiner has inadvertently omitted several such recitations of Claim 10 in his comparison of Claim 10 with Devin. While it may be true, as Examiner contends,[1] that "Devin teaches the use of a Flash memory device, and first and second memory portions for programming the device," as stated by Examiner, Applicant respectfully points out that Applicant's Claim 10 recites "**first and second Flash memory portions** each **including plural memory blocks** with **plural memory locations, each** of the memory **locations sharing an address with a corresponding memory location in each of the blocks of the first and second Flash memory portions, all of the memory locations sharing a same address being a set of memory locations**." Hence, even if it were true that "Devin teaches the use of a Flash memory device, and first and second memory portions for programming the device" as asserted

[1] The foregoing is not an admission; rather, Applicant is just using Examiner's assertion for sake of argument.

by Examiner, Devin would still not show or suggest the recitations of Applicant's Claim 10 (especially the foregoing bolded portions of Claim 10).

Applicant also respectfully points out that, while Examiner has graciously set forth the recitations of Applicant's Claim 10, Examiner has inadvertently omitted several such recitations of Claim 10 in his comparison of Claim 10 with Devin in combination with Cappelletti.. While it may be true, as Examiner contends,[2] that "[although] Devin does not expressly teach the use of pointers for reading and writing to memory locations.... [but] Cappelletti does expressly teach the use of pointers when programming the memory portions of a Flash memory device (see Col. 2, lines 50-60).... [and] It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Devin with Cappelletti because doing so optimizes the programming of flash memory devices," as stated by Examiner, Applicant respectfully points out that Applicant's Claim 10 recites "a plurality of **memory pointers** each **reflecting which memory block includes a current memory location for a set of memory locations, each set of memory locations including a current memory location**; and a **memory controller structured to**, in response to receiving a request to write data to a selected address assigned to a selected one of the sets of memory locations, **determine from a memory pointer associated with the selected address which memory location in the selected set is a next memory location following the current memory location for the selected set and write the data in the next memory location.**" Hence, even if it were true that "[although] Devin does not expressly teach the use of pointers for reading and writing to memory locations.... [but] Cappelletti does expressly teach the use of pointers when programming the memory portions of a Flash memory device (see Col. 2, lines 50-60)...." as asserted by Examiner, Devin in combination with Cappelletti would still not show or suggest the recitations of Applicant's Claim 10 (especially the foregoing bolded recitations of Claim 10).

As has been shown, Devin in combination with Cappelletti does not show or suggest many of the recitations of Applicant's Independent Claim 10 (especially the foregoing

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[2] The foregoing is not an admission; rather, Applicant is just using Examiner's assertion for sake of argument. In addition, Applicant disagrees with there being a teaching to combine Devin and Cappelletti. However, insofar as Applicant can demonstrate that no prima facie case of obviousness exists without reaching these points, Applicant reserves the right to argue against the foregoing points at a later time, should such become necessary.

bolded portions of Applicant's Independent Claim 10). Accordingly, for at least the foregoing reasons, Applicant respectfully suggests that Devin in combination with Cappelletti does not establish a prima facie case of obviousness of Applicant's Claim 10, and hence respectfully requests the Examiner withdraw his rejection and issue a Notice of Allowance for Independent Claim 10. In addition, Claims 11-15 depend either directly or indirectly from Independent Claim 10. "A claim in dependent form shall be construed to incorporate by reference all the limitations of the claim to which it refers." 35 U.S.C. § 112 paragraph 4. Consequently, Dependent Claims 11-15 are not rendered unpatentable by the art of record for at least the reasons why Independent Claim 10 is not rendered unpatentable by the art of record. Accordingly, Applicant respectfully requests that Examiner withdraw his rejections of Dependent Claims 11-15 for at least these reasons, and issue a Notice of Allowance on such dependent claims.

35 U.S.C. § 112 Rejections

Examiner has rejected Claims 1, 8, and their respective dependent claims for lack of definiteness on the basis that Applicant has used the term "predetermined number" without specifying what that number is (e.g., predetermined number of sectors, predetermined number of blocks, predetermined number of pages). *See Examiner's Office Action* p.3 (03 July 2002). Applicant respectfully points out that "breadth of a claim is not to be equated with indefiniteness. In re Miller, 441 F.2d 689, 169 USPQ 597 (CCPA 1971). If the scope of the subject matter embraced by the claims is clear, and if applicants have not otherwise indicated that they intend the invention to be of a scope different from that defined in the claims, then the claims comply with 35 U.S.C. 112, second paragraph." MPEP § 2173.04.

As evidence that the terminology of Applicant's claims is broad, rather than indefinite, Applicant respectfully points Examiner to issued U.S. Patents 6,473,879 (to Ishii); 6,473,878 (to Wei) which use the words "predetermined number" without reciting what that number is. Accordingly, Applicant respectfully asserts that Applicant's Claims 1, 8, and their respective dependent claims are not indefinite under 35 U.S.C. § 112 and hence respectfully asks that Examiner's rejections due to indefiniteness be withdrawn.

Examiner Requested Art

The Examiner has requested a few art references that are not yet in the file: an "Onwards and Upwards" article, and "specification sheets or data sheets for the versions of the ST9 Microcontroller produced in the years 1994-1997." *See Examiner's Office Action* p.3 (03 July 2002). Applicant respectfully asserts that the references requested are not materially related to the subject matter of Applicant's application, and hence are not material to patentability. Nonetheless, even though Applicant does not consider that the foregoing references are at all material to patentability, as a courtesy to Examiner, *if* Applicant can locate the specification sheets or data sheets for the versions of the ST9 Microcontroller produced in the years 1994-1997 (it is not clear at present whether such art can be located), Applicant will submit such art in a Supplemental IDS. Applicant's undersigned representative respectfully points out that at present Applicant's representative does not have copies of such art, if such art exists.

With respect to the "Onwards and Upwards" art, Applicant points out that Examiner has stated that the publication date of the "Onwards and Upwards" art is March 1999, which post-dates the foreign priority date, 30 September 1998 of Applicant's application, and hence the "Onwards and Upwards" art is not prior art to Applicant's application. Accordingly, Applicant respectfully asserts that it will not be submitting such art, unless Examiner mandates otherwise.

Examiner Questions Regarding Oath or Declaration

The Examiner has requested clarification "as to relationship of Misters Devin, Leconte, Demange, Aulas, Guedj, Cappelletti, and Maurelli to the claimed invention; therefore, Applicants provide a statement for clarification." *See Examiner's Office Action* p.4 (03 July 2002). In response, Applicant respectfully points out that there is a duly executed Declaration in the file naming Maurizio Peri, Alessandro Brigati, and Marco Olivo as inventors. Applicant sees no need to look behind the face of this duly executed declaration, and accordingly states that, on its face the duly executed declaration shows that "Misters Devin, Leconte, Demange, Aulas, Guedj, Cappelletti, and Maurelli" bear no relationship to the claimed invention.

Examiner Suggested Title

The Examiner has suggested that Applicant retitle the application to be "Flash EEPROM Memory Emulator of Non-Flash EEPROM Device and Corresponding Method." *See Examiner's Office Action* p.5 (03 July 2002). In response to Examiner, Applicant has amended the title herein.

Claim Interpretation

Examiner has set forth a proposed interpretation of "a 'Flash" memory structure" as being a "flash EEPROM" as described in Brigati, U.S. Patent 6,011,717, Col. 1, lines 24-31, [in that] Examiner interprets "Flash EPROM" as being a set of devices that include "flash EEPROM." *See Examiner's Office Action* p.5 (03 July 2002) (Brigati discloses Flash EPROM). In response to Examiner, Applicant respectfully requests that "the pending claims ... be 'given the broadest reasonable interpretation consistent with the specification'" as mandated by *MPEP* § 2113.

Claim Objection

In his Office Action, Examiner objected to informalities in the then-pending Dependent Claim 9. *See Examiner's Office Action* p.5 (03 July 2002). In response to Examiner, Applicant has amended Claim 8 to be Claim 9 rewritten in independent form, and in the process has corrected the informalities noted by Examiner.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version With Markings to Show Changes Made.**" If a conflict arises between the clean copy and the attached "**Version With Markings to Show Changes Made,**" this statement constitutes public notice that the

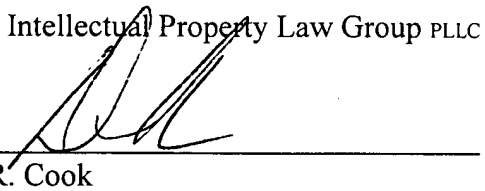
Applicant respectfully request that their intent is that the version with changes made be considered controlling, since that is the version which both the Examiner and the Applicant are considering during prosecution.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

Maurizio Peri et al.

SEED Intellectual Property Law Group PLLC



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

Please replace the title appearing on page 1 with the following title: Flash EEPROM Memory Emulator of Non-Flash EEPROM Device and Corresponding Method.

In the Claims:

Claim 8 has been amended as follows. Claim 9 has been cancelled.

8. A method for emulating features of an EEPROM memory device incorporated into a memory macrocell which is embedded into an integrated circuit that also includes a microcontroller and a Flash memory structure formed by a predetermined number of sectors, comprising using at least two sectors of the Flash memory structure to emulate EEPROM byte alterability by dividing each of said at least two sectors into a pre-determined number of blocks of the same size and each block into a pre-determined number of pages and updating the emulated EEPROM memory portion programming different memory locations in a single bit mode, wherein at a page update selected page data are moved to a next free block and, when an EEPROM sector is full, all the pages are swapped to another EEPROM sector.

9. (Cancelled) ~~The method according to claim 8, wherein at a page update selected page data are moved to a next free block and, when an EEPROM sector is full, all the pages are swapped to the another EEPROM sector.~~